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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,171	01/20/2004	Akif Sultan	50432-395	6644

7590 02/25/2005

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/759,171	SULTAN ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 1/20/04. Currently, claims 1-15 are pending.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawing submitted on 6/16/04 are informal drawings. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: On page 3, paragraph [12], line 7, "sifficient" should be spelled "sufficient". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim 9 is objected to because of the following informalities: On lines 2, "than" should be inserted after "first width greater". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al., US Patent 5,476,802.

Yamazaki discloses the semiconductor method as claimed. See figures 1(A)-8(D) with emphasis on figures 5(A)-5(C), and corresponding text, where Yamazaki teaches, pertaining to claim 1, a method of manufacturing a semiconductor device, the method comprising: forming a polysilicon gate electrode precursor **111** (pre-gate), having first side surfaces at a first width and a first upper surface at a first height, over a mean surface of the semiconductor substrate with a gate insulating layer **112** therebetween (figure 5(A); col. 4, lines 26-36); selectively oxidizing the first side surfaces and the upper surface of the polysilicon gate electrode precursor to form oxidized layers **114** thereon (figure 5(B); col. 4, lines 45-57); and removing the oxidized layer from the polysilicon gate electrode precursor to form a polysilicon gate electrode having second

side surfaces at a second width less than the first width and a second upper surface at a second height less than the first height (figure 5(C); col. 6, lines 1-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,476, 802 in view of Stanley Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era, Volume I, Lattice Press, 1986, pages 191-194.

Yamazaki discloses the semiconductor method substantially as claimed. See preceding rejection of claim 1under 35 U.S.C. 102(b). In addition, Yamazaki shows, pertaining to claim 3, the method, comprising: forming an oxide layer on the main surface of the semiconductor substrate; forming a layer of polysilicon on the on the oxide layers; patterning to form the polysilicon gate electrode precursor with a gate oxide layer thereunder and extending on the main surface of the semiconductor substrate. Also, Yamazaki shows, pertaining to claim 4, the method comprising: ion implanting impurities, using the polysilicon gate electrode precursor as a mask, to form deep source/drain regions; selectively oxidizing the side surfaces and the upper surface of the polysilicon gate electrode precursor to form the oxidized layers thereon; removing the oxidized layers from the silicon gate precursor to form the polysilicon gate electrode; and ion implanting impurities, using the polysilicon gate electrode as a mask, to form source/drain

extensions. Yamazaki shows, pertaining to claim 5, the method, further comprising: forming dielectric sidewall spacers on the side surfaces of the polysilicon gate electrode; and forming metal silicide layers on the upper surface of the polysilicon gate electrode and on the main surface of the semiconductor substrate over the deep source/drain regions. In addition, Yamazaki shows, pertaining to claim 6, the method comprising forming sidewall spacers on the side surfaces of the polysilicon gate electrode. Also, Yamazaki shows, pertaining to claims 7 and 15, the method comprising: forming an oxide liner on the second side surfaces of the polysilicon gate electrode and on a portion of the main surface of the semiconductor substrate. Finally, Yamazaki shows, pertaining to claim 14, the method comprising: forming sidewall spacers on the second side surfaces of the polysilicon gate electrode; and forming metal silicide layers on the second upper surface of the polysilicon gate electrode and on the main surface of the semiconductor substrate over the deep source/drain regions.

However, Yamazaki fails to show, pertaining to claim 2, the method comprising forming nitride layers on the main surface of the semiconductor substrate on each side of the polysilicon gate electrode precursor. In addition, Yamazaki fails to show, pertaining to claim 3, the method comprising forming the nitride layers on the gate oxide layer extending on the main surface of the semiconductor substrate. Also, Yamazaki fails to show, pertaining to claim 4, the method comprising forming the nitride layers on the main surface of the semiconductor substrate over the deep source/drain regions; and removing the nitride layers. Yamazaki fails to show, pertaining 6, the method comprising forming silicon nitride sidewall spacers as the sidewall spacers on the side surfaces of the polysilicon gate electrode. In addition, Yamazaki fails to show, pertaining to claims 7 and 15, the method comprising forming the silicon nitride sidewall

spacers on the oxide liner. Also, Yamazaki fails to show, pertaining to claim 8, the method comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500Å. Yamazaki fails to show, pertaining to claim 9, the method comprising forming the polysilicon gate electrode precursor at a first height greater than 1,000 Å and at a first width greater than 500Å. In addition, Yamazaki fail to show, pertaining to claim 10, the method comprising forming the polysilicon gate electrode at a second height of 300 Å to 900 Å and a second width of 150 Å to 400Å. Also, Yamazaki fails to show, pertaining to claim 11, the method comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500 Å. Yamazaki fails to show, pertaining to claim 12, the method comprising forming the polysilicon gate electrode precursor at a first height greater than 1000Å and at a first width greater than 500 Å. In addition, Yamazaki fails to show, pertaining to claim 13, the method comprising forming the polysilicon gate electrode at a second height of 300 Å to 900Å and at a second width of 150 Å to 400Å. Finally, Yamazaki fails to show, pertaining to claim 14, the method comprising forming silicon nitride sidewall spacers on the second side surfaces of the polysilicon gate electrode.

Wolf teaches, on pages 191-194, the conventional properties of silicon nitride used in semiconductor manufacturing of integrated circuits that includes MOSFET devices.

It would have been to one of ordinary skill in the art substitute, the method comprising forming nitride layers on the main surface of the semiconductor substrate on each side of the polysilicon gate electrode precursor; the method comprising forming the nitride layers on the gate oxide layer extending on the main surface of the semiconductor substrate; the method comprising forming the nitride layers on the main surface of the semiconductor substrate over

the deep source/drain regions; and removing the nitride layers; the method comprising forming silicon nitride sidewall spacers as the sidewall spacers on the side surfaces of the polysilicon gate electrode; the method comprising forming the silicon nitride sidewall spacers on the oxide liner; the method comprising forming silicon nitride sidewall spacers on the second side surfaces of the polysilicon gate electrode, in the method of Yamazaki, pertaining to claims 2-4, 6, 7, 14 and 15, according to the teachings of Wolf, with the motivation that, the silicon nitride material taught by Wolf, are conventionally well known for its barrier properties against diffusion, its ability to withstand severe environmental stress, coverage of metal, and deposition with acceptably low pinhole densities, resulting in a reliably useful masking layer for selective oxidation as well as for a passivation layer used as sidewall spacers.

It would have been obvious to one of ordinary skill in the art to incorporate, the method comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500Å ; the method comprising forming the polysilicon gate electrode precursor at a first height greater than 1,000Å and at a first width greater than 500Å ; the method comprising forming the polysilicon gate electrode at a second height of 300 Å to 900 Å and a second width of 150Å to 400Å ; the method comprising forming the polysilicon gate electrode at a second height less than 1,000 Å and at a second width less than 500 Å ; the method comprising forming the polysilicon gate electrode precursor at a first height greater than 1000 Å and at a first width greater than 500 Å ; the method comprising forming the polysilicon gate electrode at a second height of 300 Å to 900Å and at a second width of 150Å to 400Å , in the method of Yamazaki, pertaining to claim 8-13, according to both the teachings of Yamazaki in view of Wolf, with the motivation that, the gate electrode precursor (pre-gate) and gate electrode,

taught by Yamazaki, specifically, teaches forming an oxidation step on the gate electrode precursor, resulting in a reduced gate width and height, for the purpose of increasing the speed of the semiconductor device, making it a more efficient device. Therefore, having the above widths and height would result in routine experimentation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
February 19, 2005

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812